SigmaDSP™ 28-/56-Bit Audio Processor Evaluation Boards
EVAL-AD1940EB/AD1941EB

EVALUATION BOARD OVERVIEW

This document explains the design and setup of the AD1940/AD1941 SigmaDSP evaluation boards.

The AD1940EB/1941EB provide a full range of analog and digital inputs and outputs to and from the AD1940/AD1941. The SigmaDSP can connect to analog I/O signals through the AD1939 codec and AD1871 ADC. Digital I/O connections are available in both S/PDIF and 3-wire serial data formats. The DSP is controlled by Analog Devices' SigmaStudio™ software, which interfaces to the evaluation boards with either a USB or parallel port connection. USB control is available via the EVAL-ADUSB1 add-on board. Power is distributed by a single supply, which is regulated to the necessary voltages on the boards. The PCB is an 8" × 7 ¾" 4-layer design with split analog and digital power and ground planes on the two inner layers.

PACKAGE CONTENTS

The AD1940EB/AD1941EB packages contain these items:

- AD1940/AD1941 evaluation board
- EVAL-ADUSB1 USB adapter
- SigmaStudio software CD
- Universal power supply
- USB cable
- Evaluation board/software quick-start guide

AD1940/AD1941 DEVICE DESCRIPTION

The AD1940/AD1941 are complete 28-bit, single-chip, multichannel audio DSPs for equalization, multiband dynamic processing, delay compensation, speaker compensation, and image enhancement. These algorithms can be used to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement of perceived audio quality.
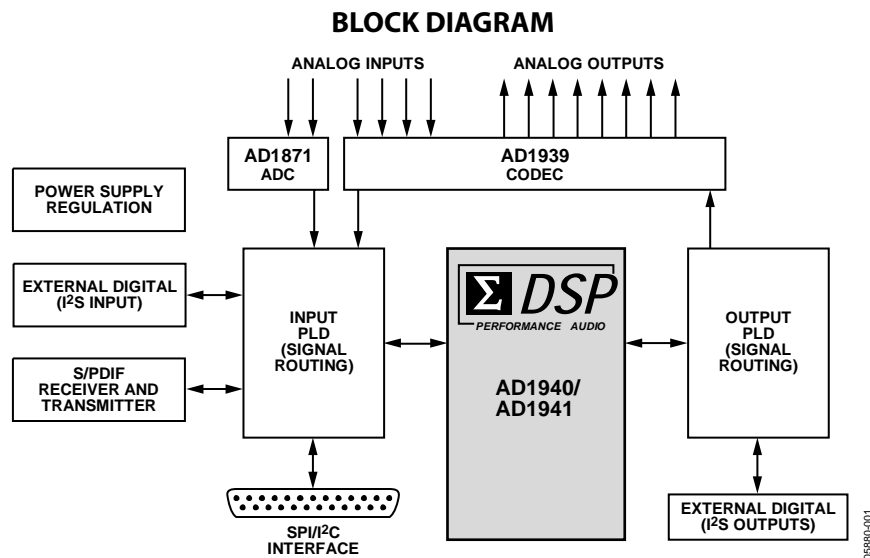
BLOCK DIAGRAM

Figure 1.

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REVISION HISTORY

1/06—Revision 0: Initial Version

AD1940/AD1941 DEVICE DESCRIPTION

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The signal processing used in the AD1940/AD1941 is comparable to that found in high end studio equipment. Most of the processing is done in full, 56-bit double-precision mode, resulting in very good, low level signal performance and the absence of limit cycles or idle tones. The dynamics processor uses a sophisticated, multiple-breakpoint algorithm often found in high end broadcast compressors.

The AD1940/AD1941 are fully-programmable DSPs. Easy-to-use software allows the user to graphically configure a custom signal processing flow, using blocks such as biquad filters, dynamics processors, and surround sound processors. An extensive control port allows click-free parameter updates, along with readback capability from any point in the algorithm flow.

The digital input and output ports of the AD1940/AD1941 allow a glueless connection to ADCs and DACs by multiple, 2-channel serial data streams or TDM data streams. When in TDM mode, the AD1940/AD1941 can input 8 channels or 16 channels of serial data, and can output either 8 channels or 16 channels of serial data. The input and output port configurations can be set individually. The AD1940 is controlled via a 4-wire SPI® port; the AD1941 is controlled by a 2-wire I²C bus.

SETTING UP THE EVALUATION BOARDS

POWER SUPPLY

The AD1940EB/AD1941EB are powered by a single supply through Coax Power Jack J14. The supply should be 9 V to 12 V dc with the ability to source at least 700 mA. The connector's polarity should be tip positive. This single supply is regulated to separate 5 V analog and digital planes. The AD1940/AD1941 and AD1939 generate 2.5 V and 3.3 V, respectively, from the 5 V supply using their on-board regulators.

DIGITAL AUDIO INPUTS AND OUTPUTS

Digital audio I/Os can be connected to the boards in two different formats. First, the evaluation boards can input or output a standard 2-channel S/PDIF stream. These I/Os can be either electrical (Jack J1 and Jack J2) or optical (Fiber Optic Modules U1 and U5). The input S/PDIF source is selected with SW10. Both S/PDIF transmit streams are always on. The S/PDIF I/O streams are connected to SDATA_IN0 and SDATA_OUT0 and are active according to the specific switch settings shown in Table 2 and Table 3.

Second, the digital audio I/O connections are in the 3-wire I²S format. Input Header J11, Output Header J7, and Output Header J8 can connect to external ADCs, DACs, and codecs with an I²S left-justified or right-justified data stream. Master clock, left/right clock, and bit clock connections are also on these headers. Up to four stereo audio streams can be input or output on each of these headers. These audio streams, when selected by the rotary mode switches, interface directly to the serial data ports of the AD1940/AD1941. These headers also serve as the I/Os for the multichannel TDM streams.

ANALOG AUDIO INPUTS AND OUTPUTS

The evaluation boards can input six analog audio signals and can output eight signals. The converters connected to the AD1940/AD1941 SigmaDSP are a 4 ADC/8 DAC AD1939 and an AD1871 stereo ADC. The full-scale I/O voltage on these connections is 1 V rms.

RCA Jack J18 to Jack J20 are the inputs to the ADCs.

RCA Jack J3 to Jack J6 and mini Jack J12, mini Jack J15, and mini Jack J16 are the DAC output connectors. The output is low-pass filtered with an anti-image filter and converted from a differential voltage output to single-ended voltage by op-amps U28 to U31. The filters' −3 dB cutoff frequency is 100 kHz and has an approximate third order Bessel (linear phase) response.

CONTROL INTERFACE

PCB Connector J17 is the connection for the SPI and I²C control signals. The AD1940EB/AD1941EB typically connect to the SigmaStudio design tools with the EVAL-ADUSB1 USB adapter board. This board connects to the PC's USB port and outputs either SPI or I²C commands to the AD1940EB/AD1941EB. The USB adapter is provided with the evaluation boards, or is available for standalone use in a target system. The AD1940EB/AD1941EB can also connect directly to a PC's parallel port through PCB Connector J17, although this isn't the recommended control interface. The software connection is further explained in the Evaluation Board Software section.

SWITCH AND JUMPER FUNCTIONS

The AD1940EB/AD1941EB have many switch and jumper settings, but for most uses, many of these need to be set only once and can be ignored after that. Table 1 shows the function of each jumper and switch on the evaluation boards. For switch package S1, logic high (1) is up (assuming analog inputs are at the top of the boards) and logic low (0) is down. Jumper J21 provides a +20 dB gain in Position A and a +40 dB gain in Position B.

The functions for SW2 and SW9 are explained in more detail in Table 2 and Table 3.

Table 1. Switches and Jumpers

Reference Designator	Function
S1-1	Set PLL_CTRL0
S1-2	Set PLL_CTRL1
S1-3	Set PLL_CTRL2
S1-4	Set ADR_SEL
SW2	Input mode select
SW9	Output mode select
SW6 to SW8	Set direction (I/O) of external MCLKs
LK5/LK14	Select which signal is sent to AD1940/AD1941 PLL
LK1	Connects/disconnects MCLK input to AD1939
LK2/LK3	Connect/disconnect 12.288 MHz crystal from AD1939's oscillator circuit
J24	Select microphone or line input to AD1871 left channel
LK4	Enables/disables phantom power for microphone input
SW10	Selects between RCA and optical S/PDIF input
J21	Sets microphone gain to +20 dB or +40 dB

ROTARY SWITCH SETTINGS

SW2 and SW9 are hex rotary switches that control the input and output signal routing on the evaluation boards. The position of these switches controls which serial data signals and clocks are routed to and from the AD1940/AD1941. Table 2 shows the settings of Rotary Switch SW2. This switch controls the routing of signals to the AD1940/AD1941 (U1) serial input port. Table 2 indicates which serial data signals are sent to each of the four serial data inputs, as well as the clock source. If "slave" is indicated as the clock source, the LRCLK and BCLK signals are fed to input CPLD U13 from a source connected to output CPLD U15. An "x" in the table indicates that no signal is sent to the input pin on U1 in that mode. Switch Position A to Switch Position F are unused.

Table 3 shows the settings of Rotary Switch SW9. This switch controls the routing of the signals out of the AD1940/AD1941 (U1) serial output ports. Table 3 indicates where the serial data outputs are sent, as well as the source of the LRCLK and BCLK signals. If "slave" is indicated as the clock source, the LRCLK and BCLK signals are fed to output CPLD U15 from a source connected to input CPLD U13. An "x" in the table indicates that no signal is output from the pin on U1 in that mode. Switch Position F of SW9 is unused.

Table 2. SW2 Settings

SW2 Position	SDATA_IN0	SDATA_IN1	SDATA_IN2	SDATA_IN3	Clock Source
0	S/PDIF	1939 ADC1/2	1939 ADC3/4	Ext In 0	S/PDIF master
1	1939 ADC1 and ADC2	1939 ADC3/4	1871	Ext In 0	1871 master
2	S/PDIF	Ext In 0	Ext In 1	Ext In 2	Ext In master
3	1939 ADC1 and ADC2	1939 ADC3/4	Ext In 0	Ext In 1	Slave
4	1939 ADC1 and ADC2	1939 ADC3/4	Ext In 0	S/PDIF	1939 ADC master
5	Ext In 0	Ext In 1	Ext In 2	Ext In 3	Ext In master
6	Ext In 0	Ext In 1	Ext In 2	Ext In 3	Slave
7	x	x	1939 (TDM)	x	1939 master
8	x	x	Ext In 2 (TDM)	Ext In 3 (TDM)	Ext In master
9	x	x	Ext In 2 (TDM)	Ext In 3 (TDM)	Slave

Table 3. SW9 Settings

SW9 Position	SDATA_OUT0	SDATA_OUT1, SDATA_OUT2, SDATA_OUT3	SDATA_OUT4	SDATA_OUT5, SDATA_OUT6, SDATA_OUT7	S/PDIF Tx	O/P 0 Clock Source	O/P 1 Clock Source
0	AD1939 DAC1 and AD1939 DAC2 Ext Out 0	AD1939 DAC3 to DAC 8 Ext Out 1 to Ext Out 3	Ext Out 4	Ext Out 5 Ext Out 6 Ext Out 7	SDATA_OUT0	Slave	Slave
1	AD1939 DAC1 and AD1939 DAC2 Ext Out 0	AD1939 DAC3 to DAC 8 Ext Out 1 to Ext Out 3	Ext Out 4	Ext Out 5 Ext Out 6 Ext Out 7	SDATA_OUT0	AD1939 DAC Master	AD1939 DAC Master
2	AD1939 DAC1 and AD1939 DAC2 Ext Out 0	AD1939 DAC3 to DAC 8 Ext Out 1 to Ext Out 3	Ext Out 4	Ext Out 5 Ext Out 6 Ext Out 7	SDATA_OUT0	AD1940/AD1941 Out 0	AD1940/ AD1941 Out 0
3	AD1939 DAC1 and AD1939 DAC2 Ext Out 0	AD1939 DAC3 to DAC 8 Ext Out 1 to Ext Out 3	Ext Out 4	Ext Out 5 Ext Out 6 Ext Out 7	SDATA_OUT0	AD1940/AD1941 Out 1	AD1940/ AD1941 Out 1
4	AD1939 DAC1 and AD1939 DAC2 Ext Out 0	AD1939 DAC3 to DAC 8 Ext Out 1 to Ext Out 3	Ext Out 4	Ext Out 5 Ext Out 6 Ext Out 7	SDATA_OUT0	Ext Out 0 Master	Ext Out 0 Master
5	AD1939 DAC1 and AD1939 DAC2	AD1939 DAC3 to DAC 8	Ext Out 4	Ext Out 5 Ext Out 6 Ext Out 7	SDATA_OUT0	AD1940/AD1941 Out 0	AD1940/41 Out 1
6	AD1939 DAC1 and AD1939 DAC2	AD1939 DAC3 to DAC 8	Ext Out 4 (TDM8)	x	SDATA_OUT0	AD1939 DAC	Slave
7	AD1939 DAC1 and AD1939 DAC2	AD1939 DAC3 to DAC 8	Ext Out 4 (TDM8)	x	SDATA_OUT0	Ext Out 0 Master	Ext Out 1 Master
8	Ext Out 0	Ext Out 1 to Ext Out 3	Ext Out 4 (TDM8)/1939	x	SDATA_OUT0	Ext Out 0 Master	Ext Out 1 Master
9	Ext Out 0 (TDM16)	x	x	x	x	Ext Out 0 Master	Ext Out 0 Master
A	Ext Out 0 (TDM8)	x	Ext Out 4 (TDM8)/1939	x	x	Slave	Slave
B	Ext Out 0 (TDM8)	x	Ext Out 4 (TDM8)/1939	x	x	AD1940/AD1941 Out 0	AD1940/ AD1941 Out 1
C	Ext Out 0 (TDM8)	x	Ext Out 4 (TDM8)/1939	x	x	AD1940/AD1941 Out 0	Slave
D	Ext Out 0 (TDM8)	x	Ext Out 4	Ext Out 5 Ext Out 6 Ext Out 7	SDATA_OUT4	AD1940/AD1941 Out 0	AD1940/ AD1941 Out 1
E	Ext Out 0 (TDM8)	x	Ext Out 4	Ext Out 5 Ext Out 6 Ext Out 7	SDATA_OUT4	Ext Out 0 Master	Ext Out 1 Master

IC FUNCTIONS

Table 4 explains the function of each IC on the evaluation boards. The two large Lattice CPLDs (U13 and U15) are used only for routing signals on the board and do not perform decoding or signal conditioning.

Table 4. IC Functions

Reference Designator	Function
U1	AD1940/AD1941 SigmaDSP audio processor
U10	AD1939 4 ADC/8 DAC audio codec
U9	AD1871 stereo ADC
U13, U15	Lattice M4A5-128/64 CPLDs for signal routing
U14, U17 to U20, U26 to U31	AD8606 dual op amps for analog audio I/O buffering
U11	ADP3303-5 LDO Regulator, 5.0 V analog supply
U8	LM317AT, 5.0 V digital supply
U12	ADM811 reset generator
U32, U33	74HC125 for external MCLK I/O buffering
U3	74HC04 for driving LEDs
U22	74HC541 for buffering SPI signals
U2	CS8414 S/PDIF receiver
U4	CS8404 S/PDIF transmitter

LED FUNCTIONS

The four LEDs on the evaluation boards are useful components that indicate the boards are properly powered and set up. Table 5 explains what each LED indicates.

Table 5. LED Functions

Reference Designator	Function
D1	When lit, U2 is receiving no data, or an invalid S/PDIF stream.
	When dim, U2 is receiving valid S/PDIF data.
D2	When lit, the SPI or I²C connection is inactive.
	When dim, an SPI or I²C connection has been established.
	When blinking, an SPI or I²C transaction is occurring.
D6	Indicates +5 V DV_{DD}
D11	Indicates +5 V AV_{DD}

RESET

The AD1940EB/1941EB can be reset with push-button switch SW1. This reset signal is debounced by the ADM811 (U12). This reset signal affects the AD1940/AD1941, AD1939, AD1871, and S/PDIF receiver and transmitter. The boards can also be reset by disconnecting the power. After reset, the AD1940EB/AD1941EB do not pass audio and a control port write has to be performed so that signals are output again. See the Using SigmaStudio section for additional information.

AD1940EB/AD1941EB DIFFERENCES

The main difference between the AD1940EB and AD1941EB is the control port. The AD1940EB uses an SPI control port, whereas the AD1941EB uses an I²C port. The same PCB is used for both assemblies, with slight modifications. To accommodate for I²C communication, the AD1941EB's CPLDs have slightly different programs than those of the AD1940EB. Also, the AD1941EB has Resistor R56, Resistor R57, Resistor R72, and Resistor R73, while the AD1940EB does not.

TYPICAL SETUPS

6-CHANNEL ANALOG INPUT/ OUTPUT

Input comes from the 6-channel analog inputs to the AD1940/AD1941 SDATA_IN0 pin, SDATA_IN1 pin, and SDATA_IN2 pin, and outputs on whichever outputs (SDATA_OUTx) are designed in the SigmaStudio software. Default outputs for the input are SDATA_OUT0, SDATA_OUT1, and SDATA_OUT2, or Analog Output 0 to Analog Output 5.

In this setup, the AD1939's oscillator connected to a 12.288 MHz crystal generates the master clock. The AD1871 is the serial data clock master, and the AD1939's and AD1940/AD1941's serial data ports are slaves. Table 6 explains how the switches and jumpers need to be set up for this mode. Any component setting not mentioned in this table can be considered as "don't care."

Table 6. Evaluation Board Settings for Analog I/O

Component	Setting
SW2	Position 1
SW9	Position 0
LK1	Disconnected
LK2/LK3	Connected
LK5/LK14	AD1939
J24	Line
S1	Position 2 up (1), all other positions down (0)

S/PDIF INPUT/ANALOG AND S/PDIF OUTPUT

Input comes from the stereo S/PDIF receiver to the AD1940/AD1941 SDATA_IN0 pin and outputs on whichever outputs (SDATA_OUTx) are designed in the SigmaStudio software. Default outputs for the input are SDATA_OUT0, or Analog Output 0 or Analog Output 1. SDATA_OUT0 is also sent to the S/PDIF transmitter.

In this setup, the master clock and serial data clocks are generated by the CS8414. Table 7 explains how the switches and jumpers need to be set up for this mode. Any component setting not mentioned in this table can be considered as "don't care."

Table 7. Evaluation Board Settings for S/PDIF Input/Analog and S/PDIF Output

Component	Setting
SW2	Position 0
SW9	Position 0
LK1	Connected
LK2/LK3	Disconnected
LK5/LK14	S/PDIF
SW10	Selects S/PDIF source from either optical or RCA
S1	Position 2 up (1), all other positions down (0)

SERIAL DATA INPUT/OUTPUT

This mode is intended to be used to connect to external devices, such as ADCs, DACs, or compressed audio (such as AC-3) decoders. Input comes from the external Input Header J11 and feeds the AD1940/AD1941 SDATA_IN0 pin, SDATA_IN1 pin, SDATA_IN2 pin, and SDATA_IN3 pin. Output is on Output Header J7 and Output Header J8. The specific output pins (SDATA_OUTx) are designated in the SigmaStudio software. The signals on these headers are directly connected to the AD1940/AD1941 using I²S, left-justified, or right-justified modes. Default outputs for the input are SDATA_OUT0, SDATA_OUT1, SDATA_OUT2, and SDATA_OUT3, or Analog Output 0 to Analog Output 5. If the master clock is to be output on Output Header J7, a second jumper needs to be placed on Jumper LK5/LK14 at Position Intf-Out0. For the master clock to be output on Output Header J8, an additional jumper must be placed in Position Intf-Out. In order to avoid multiple clocks driving the MCLK line, ensure that SW6 to SW8 are set properly before placing these jumpers.

In this setup, the master clock and serial data clocks are generated by the external source.

Table 8 explains how the switches and jumpers need to be set up for this mode. Any component setting not mentioned in this table can be considered as "don't care."

Table 8. Evaluation Board Settings for Serial Data I/O

Component	Setting
SW2	Position 5
SW9	Position 0
LK1	Connected
LK2/LK3	Disconnected
LK5/LK14	Intf-In
SW6	In (down)
SW7	Out (right), if the master clock is to be output on the serial data headers
SW8	Out (left), if the master clock is to be output on the serial data headers
S1	Position 2 up (1), all other positions down (0)

EVALUATION BOARD SOFTWARE

SIGMASTUDIO SOFTWARE INTERFACE

The AD1940/AD1941 SigmaDSP is controlled by Analog Devices' SigmaStudio software. This software allows the developer to graphically build a fully customized audio signal processing flow. SigmaStudio generates run-time DSP code that is downloaded to the SigmaDSP through its SPI or I²C control port. This connection on the evaluation board is DB25 PCB Connector J17. This connector allows the SigmaDSP to connect to a PC running SigmaStudio by either USB, Analog Devices' EVAL-ADUSB1 adapter, or directly to a parallel port. Both SPI and I²C communications can be used with the USB adapter, but only SPI can be used with the parallel port.

INSTALLING SIGMASTUDIO

The evaluation board cannot be run with a PC until the SigmaStudio software has been installed. SigmaStudio must be installed on a PC running Microsoft® Windows® 2000 or Windows XP.

Follow theses steps to properly install the software and drivers.

1. Insert the **SigmaStudio CD** and browse the disc.

2. Double-click **dotnetfx.exe** to install Microsoft .NET Framework version 1.1.

   .NET installation can be skipped if version 1.1 or newer has already been installed from either www.windowsupdate.com or http://www.microsoft.com/net/

3. Double-click **setup.exe** and follow the prompts to install SigmaStudio.

4. Restart the PC if this is the first time installing SigmaStudio. You must restart the PC for the parallel port driver to function.

If the evaluation board is being used only with a parallel port control connection, you can skip the USB adapter installation located in the Configuring the Board section.

CONFIGURING THE BOARD

The EVAL-ADUSB1 (USB Adapter) allows SigmaStudio to control the evaluation board through the PC's USB port. The USB adapter is powered with +5 V through the USB port. Using the USB adapter is preferred over the parallel connection because of its faster control port speed. The AD1941EB can only be controlled with the USB adapter because the PC's parallel port cannot run as a true I²C port.

Follow these steps to set up the USB adapter on a PC.

1. Plug the USB adapter into the evaluation board's PCB Connector J17.

2. Connect the USB cable to your computer and the USB serial converter.

3. For Windows 2000: When prompted for drivers, click **Search for a suitable driver** and then click **Next**. Select **Specify a location** and deselect the other options. Click **Next**.

4. For Windows XP: When prompted for drivers, click **Install from a list or a specific location**. Click **Search for the best driver in these locations**. Select **Include this location in the search.**

5. Click **Browse** and find the **ftd2xx.inf** file in the **USB drivers** subdirectory of your SigmaStudio installation. By default, this location is **C:\Program Files\Analog Devices Inc\Sigma Studio\USB drivers**.

6. In Windows XP, if you are prompted with a message that the software hasn't passed Windows Logo testing, click **Continue Anyway.**

The USB adapter and SigmaStudio software can also be used separately from the evaluation board in a target SigmaDSP-based system. In this case, the tools should be set up as if they were connecting to the evaluation board and the USB adapter still outputs SPI or I²C signals that can interface to the target SigmaDSP. Table 9 shows the necessary pins to connect to the USB adapter in a target system. This setup is useful for real-time debugging, or for tuning a program or parameters in the actual target system. The USB adapter board can be ordered separately from the evaluation board if more are needed. One USB adapter board is provided with each evaluation board. The USB adapter schematic is shown in Figure 19.

Table 9. USB Adapter Signal Pins

Pin No.	Signal
2	CCLK (SPI), SCK (I²C)
3	CLATCH_AD1940/41
4	CDATA
9	SDA
13	COUT
18 to 25	Ground

USING SIGMASTUDIO

The AD1940/AD1941 do not pass an audio signal on power-up. First, the user must write to Bit 9 of the DSP core control register that allows data to pass from input to output. This procedure can be done manually. Bit 9 is always set to 1 after the program and parameter loading procedure is completed by clicking the **Link-Compile-Download** button in SigmaStudio. Refer to the software's online help document for additional information about using SigmaStudio with the AD1940EB/AD1941EB.

Software updates are provided via Analog Devices' FTP site. Please e-mail SigmaDSP@analog.com for login information.

SCHEMATICS
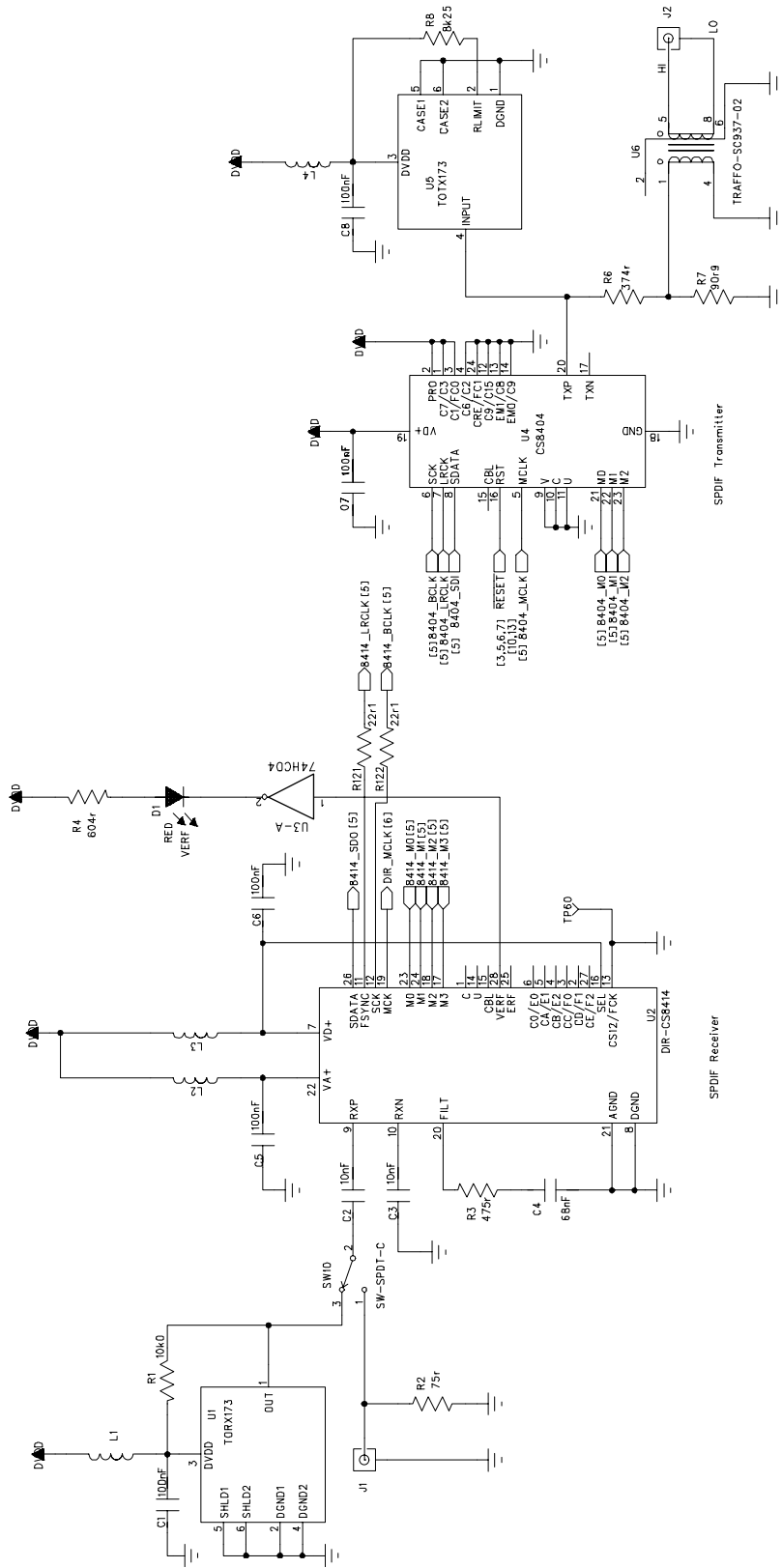
Figure 2. S/PDIF Receiver and Transmitter
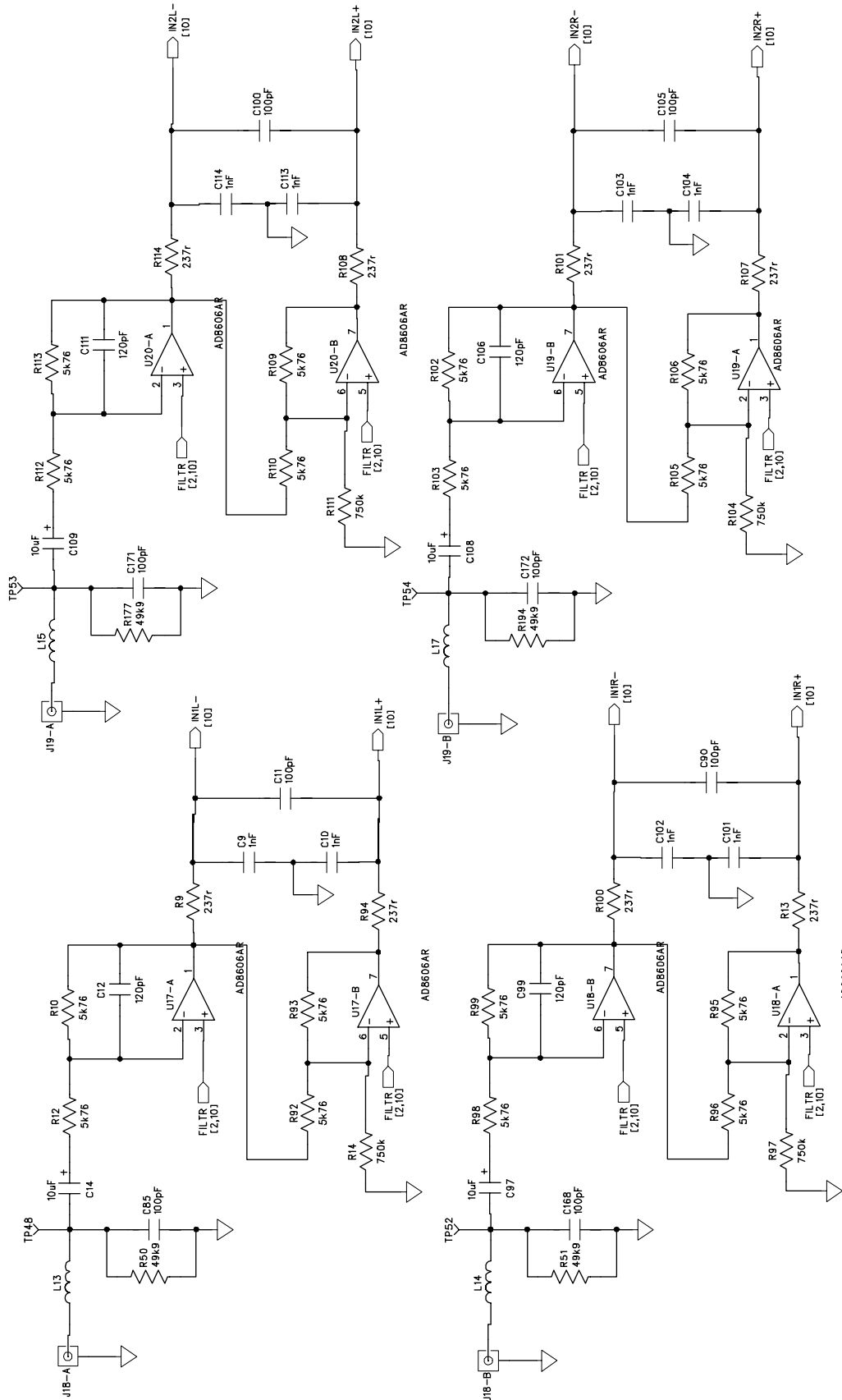
Figure 3. AD1939 Analog Input Filters
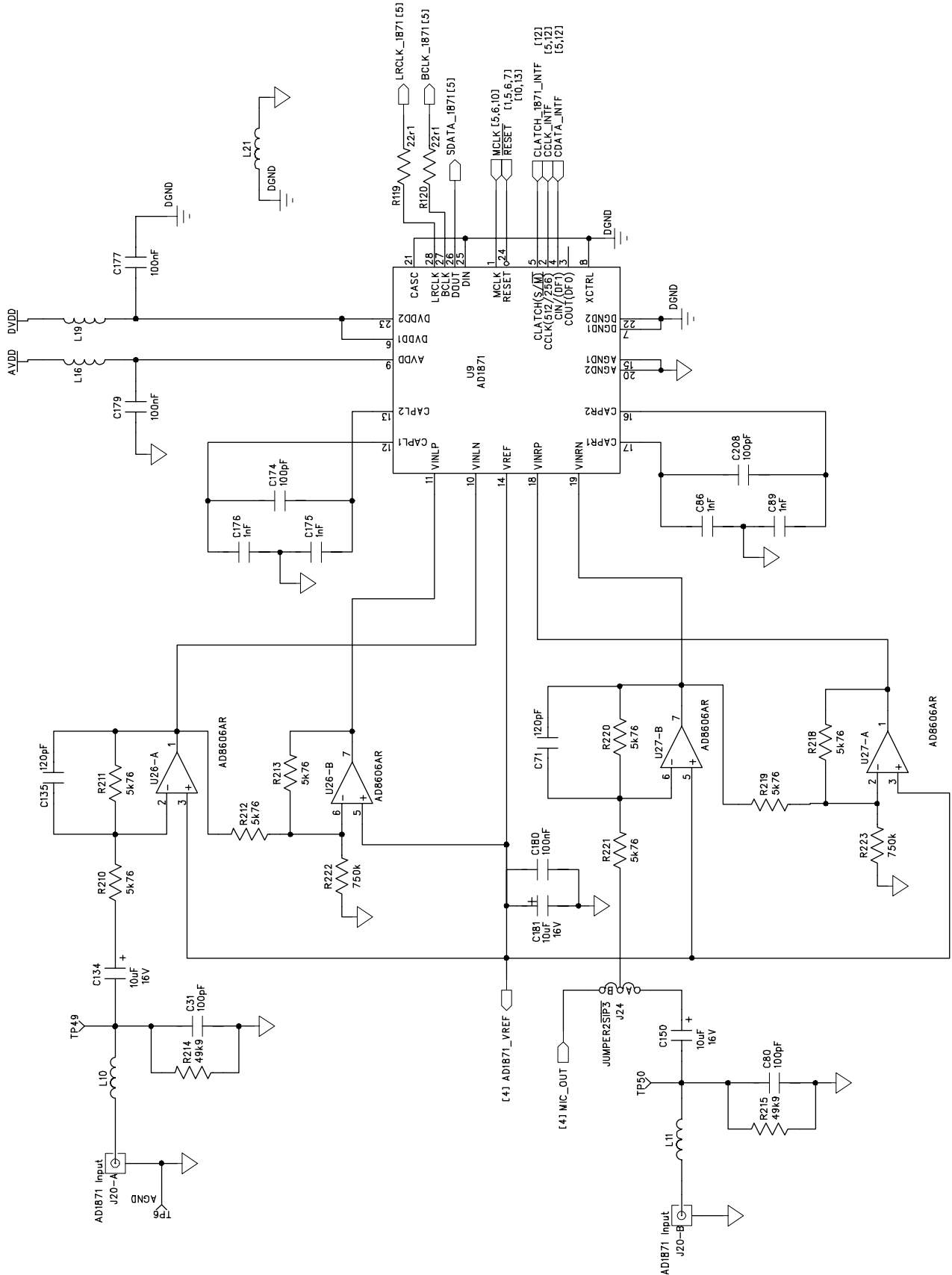
Figure 4. AD1871 Analog Input
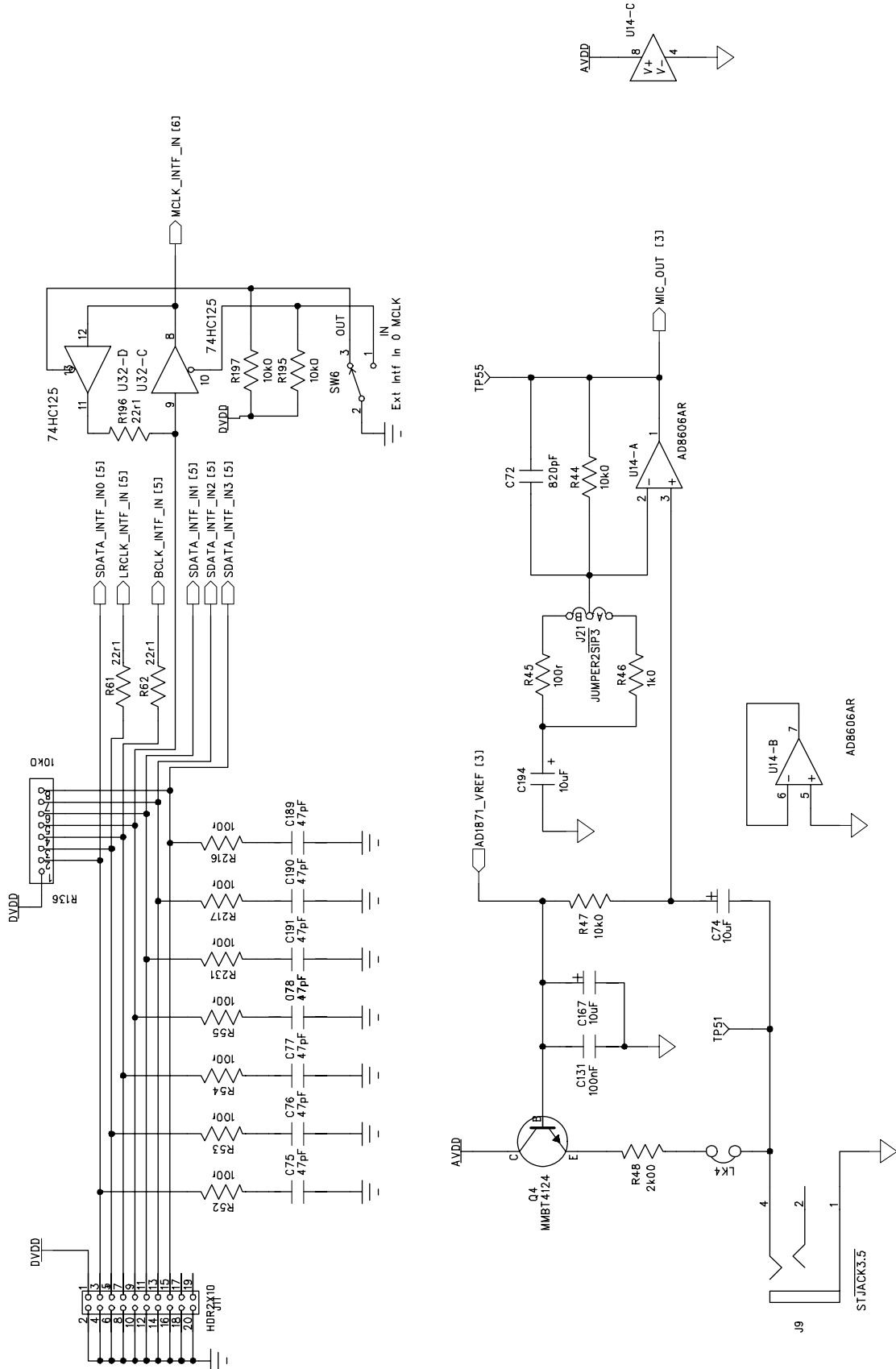
Figure 5. External Digital Inputs and Microphone Input
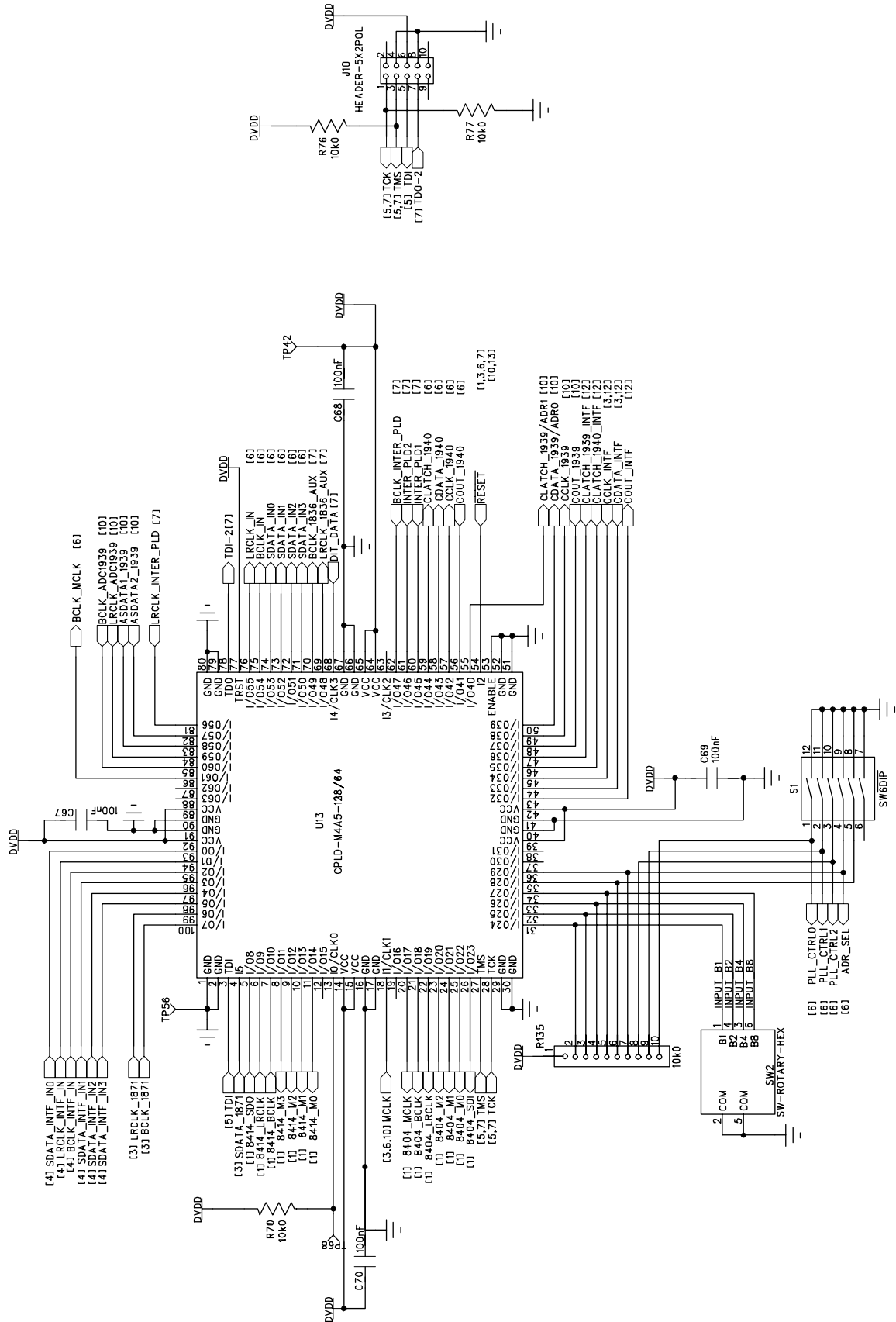
Figure 6. Input CPLD
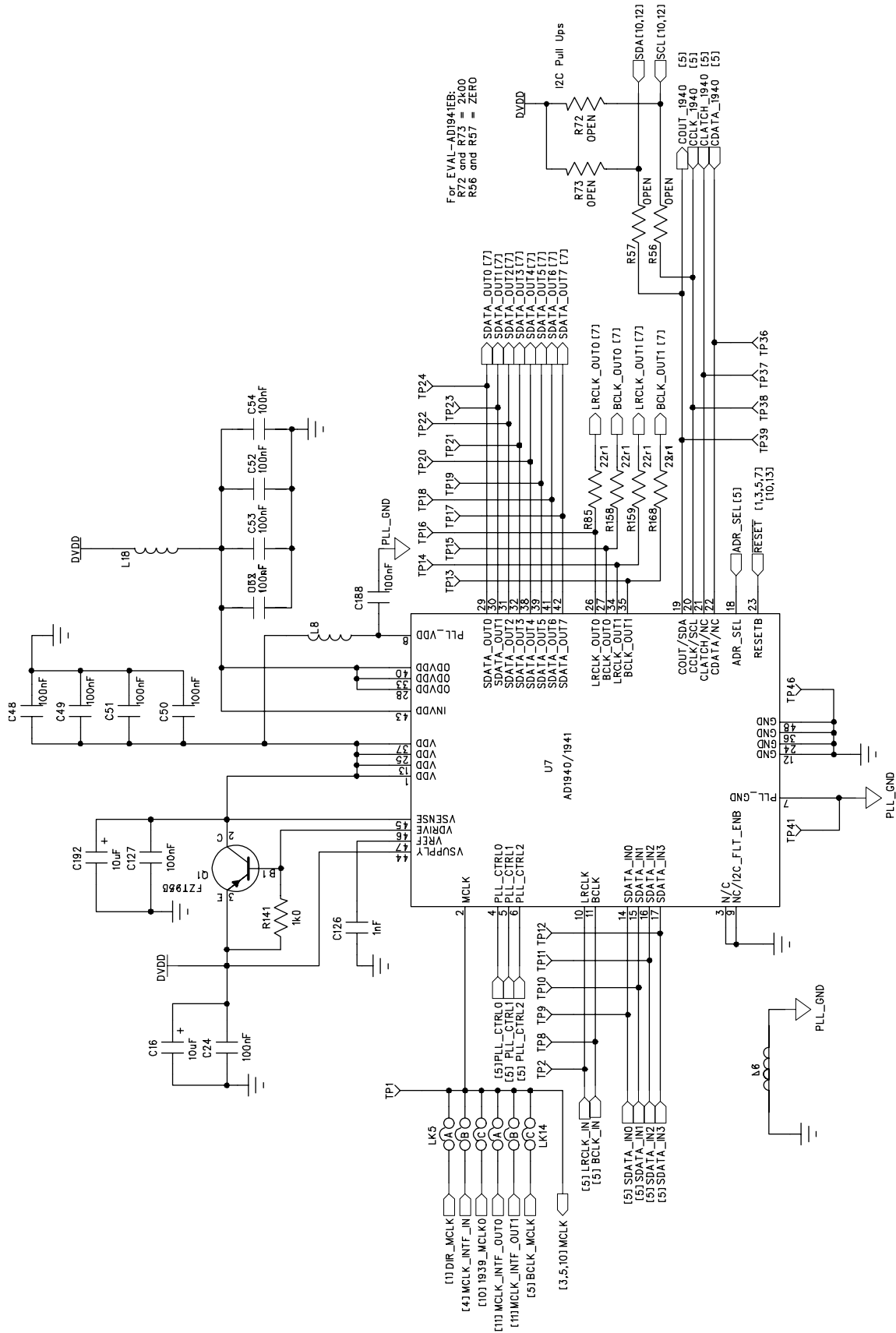
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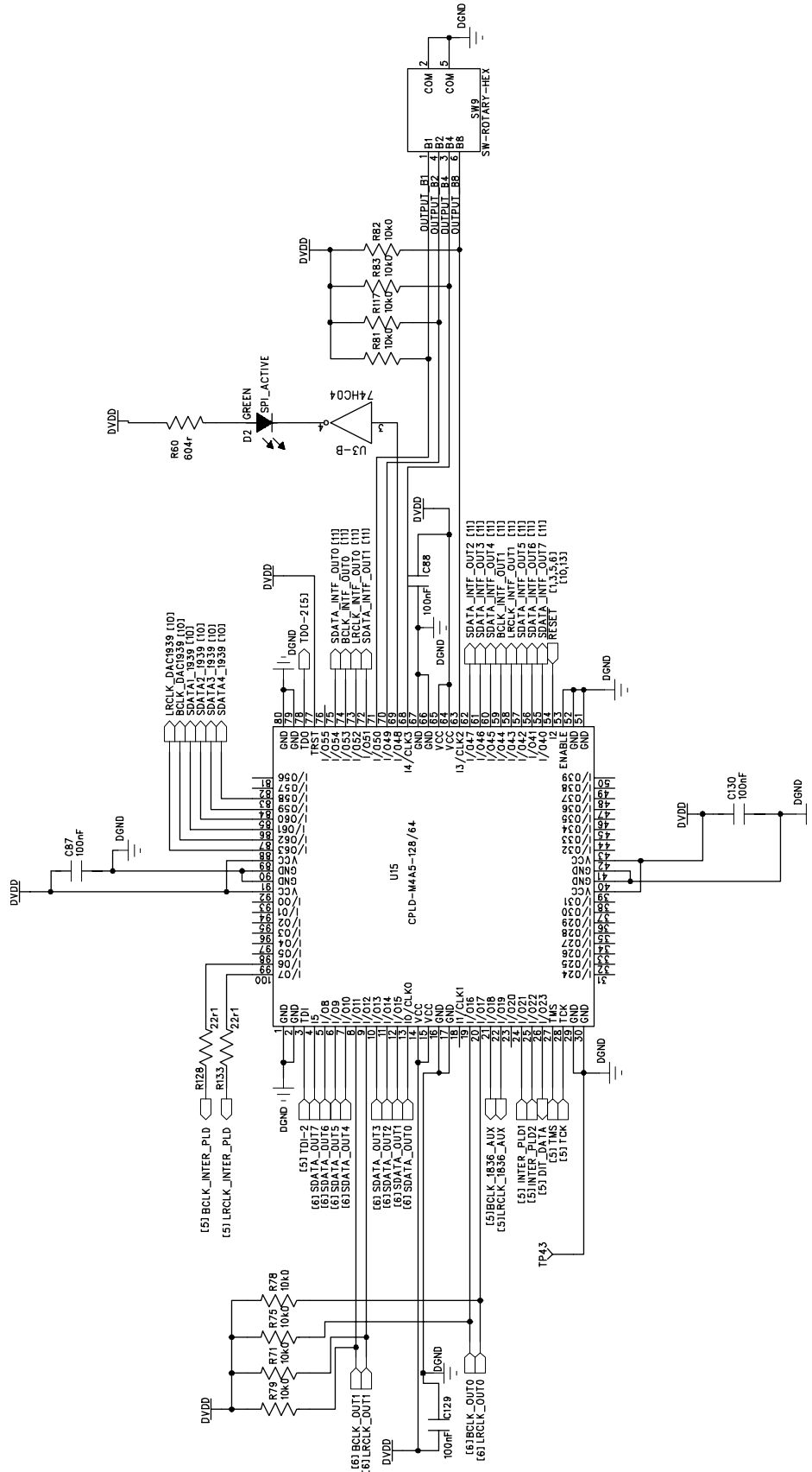
Figure 8. Output CPLD
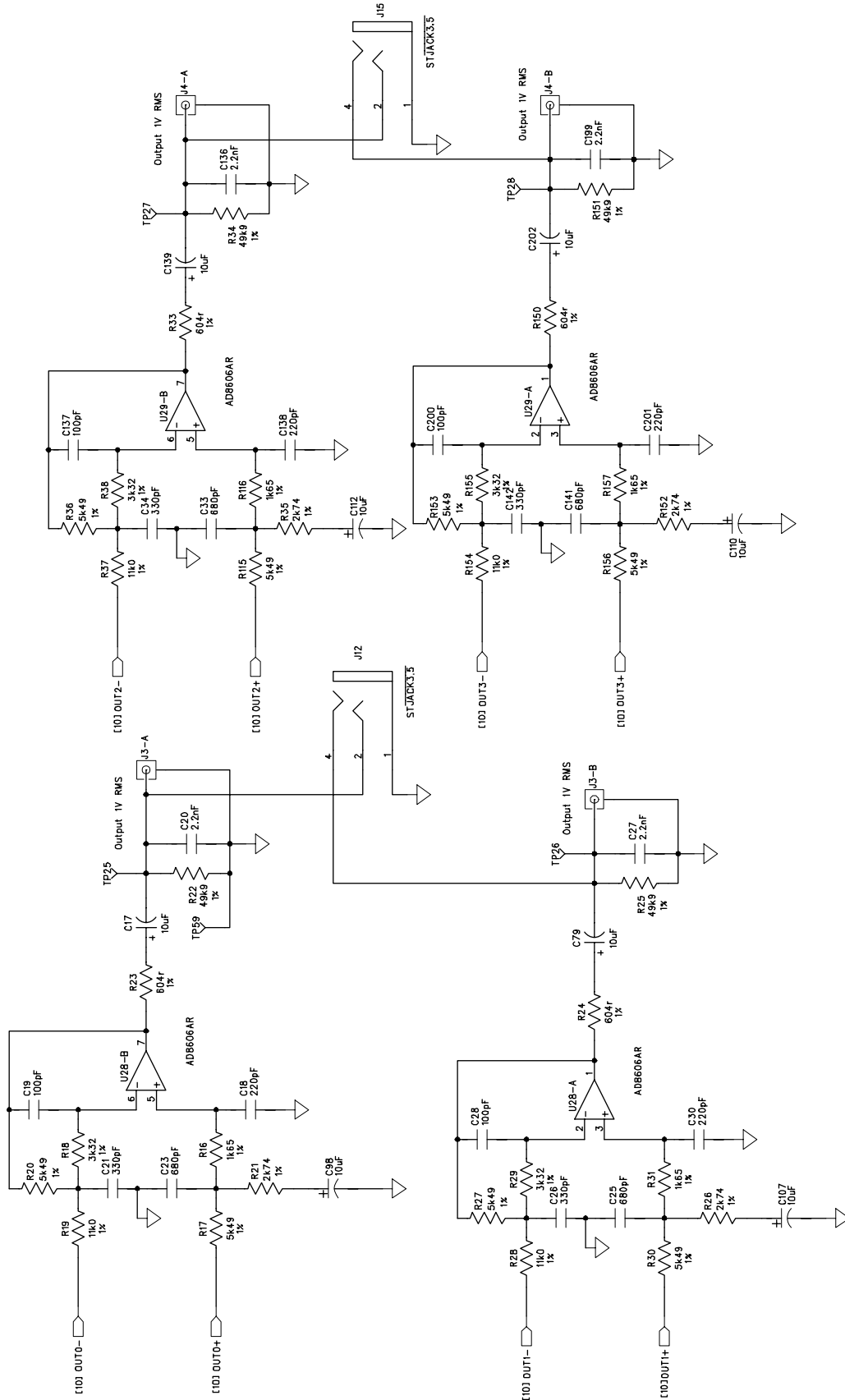
Figure 9. Analog Output 0 to Analog Output 3
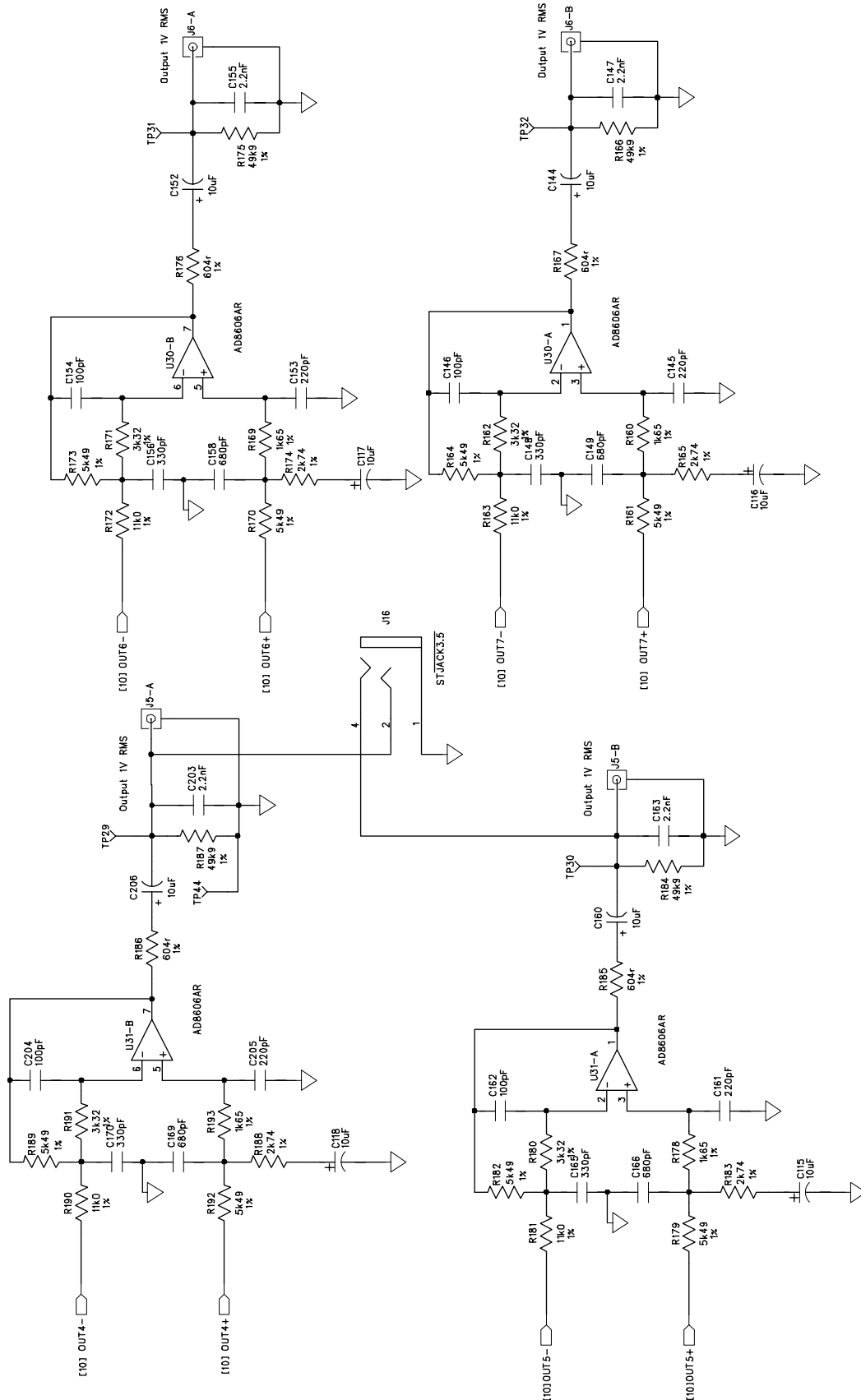
Figure 10. Analog Output 4 to Analog Output 7
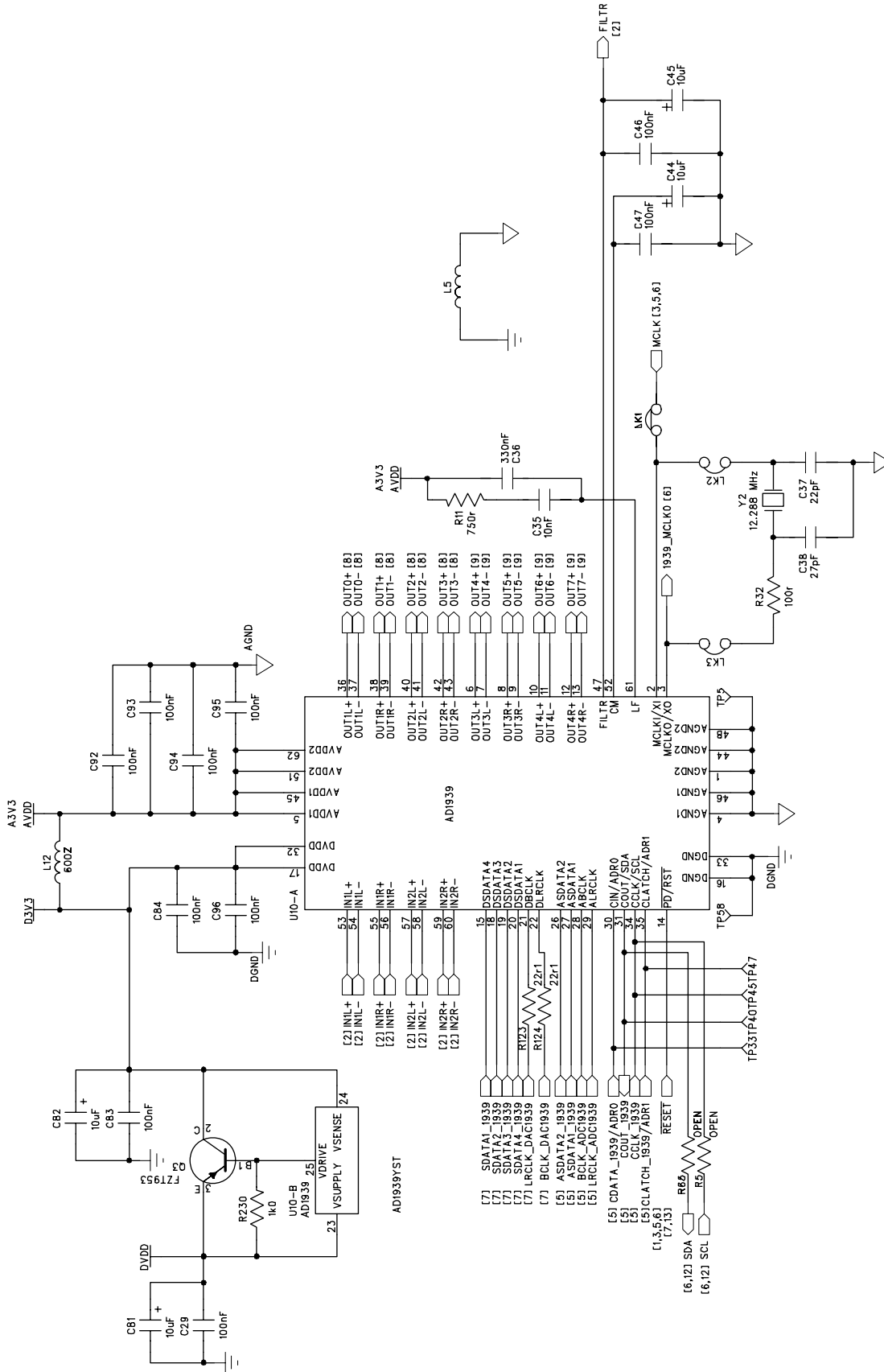
Figure 11. AD1939 Codec
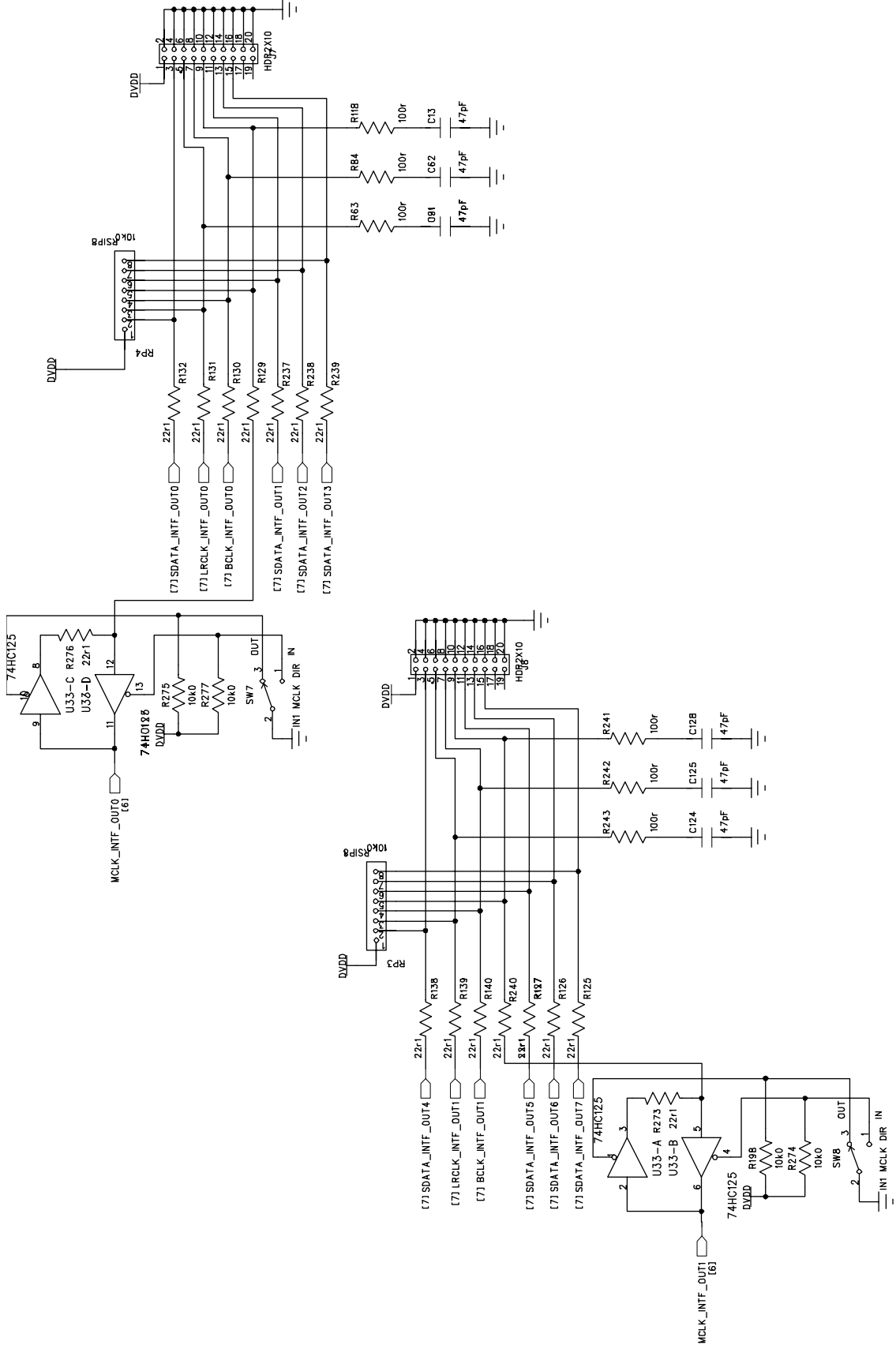
Figure 12. External Digital Outputs
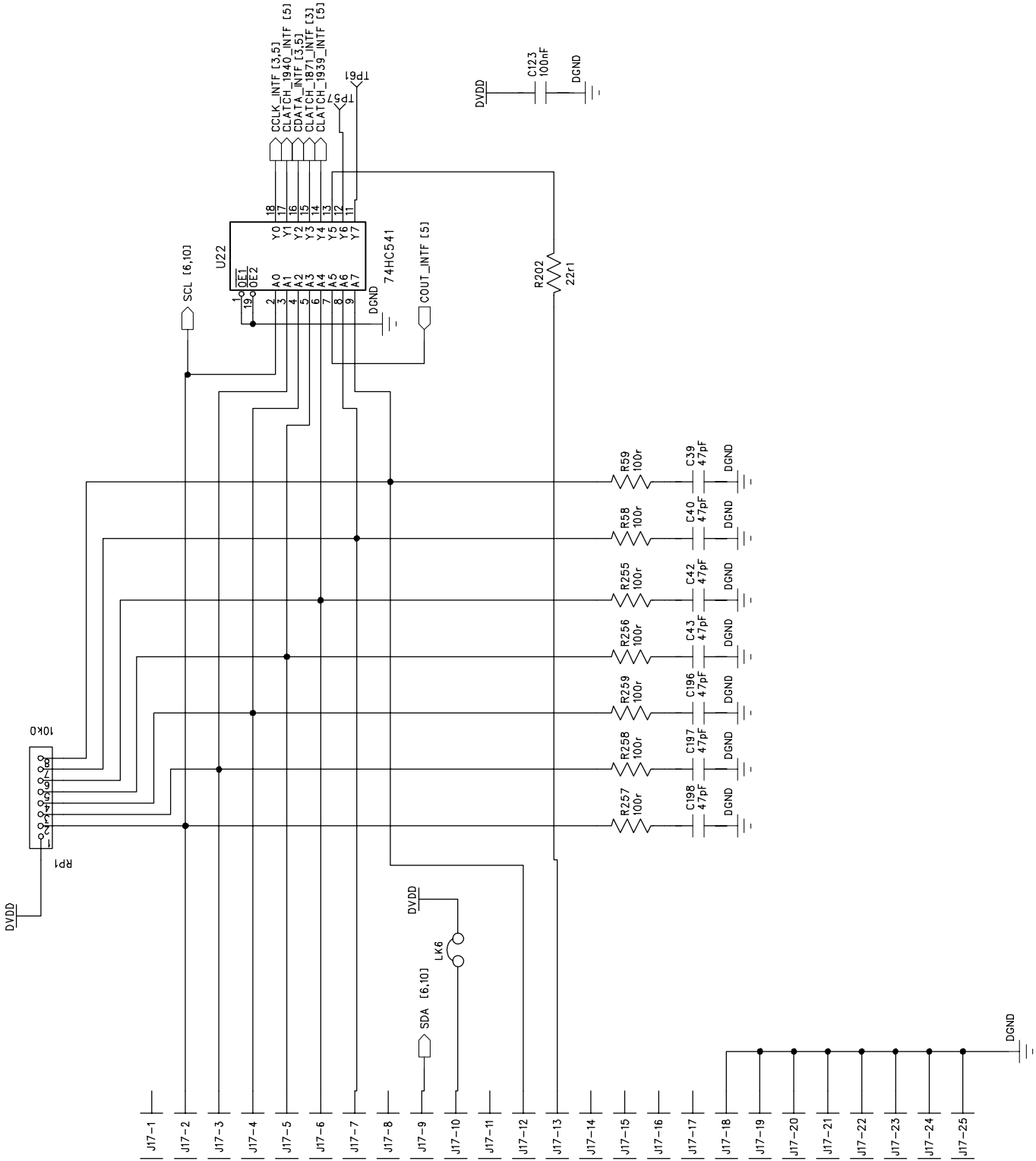
05880-012

Figure 13. SPI/I²C Control Interface
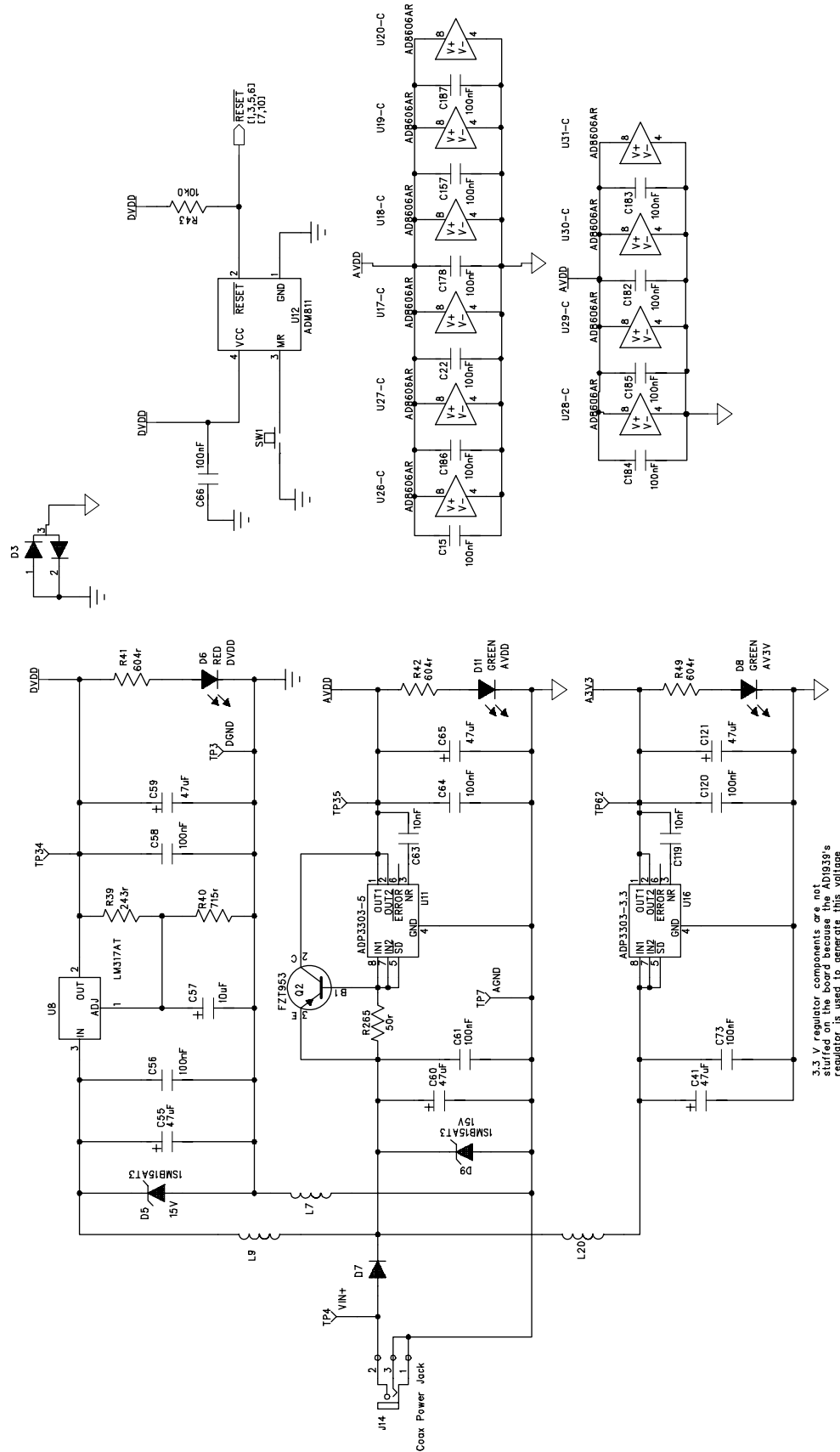
Figure 14. Power Supply

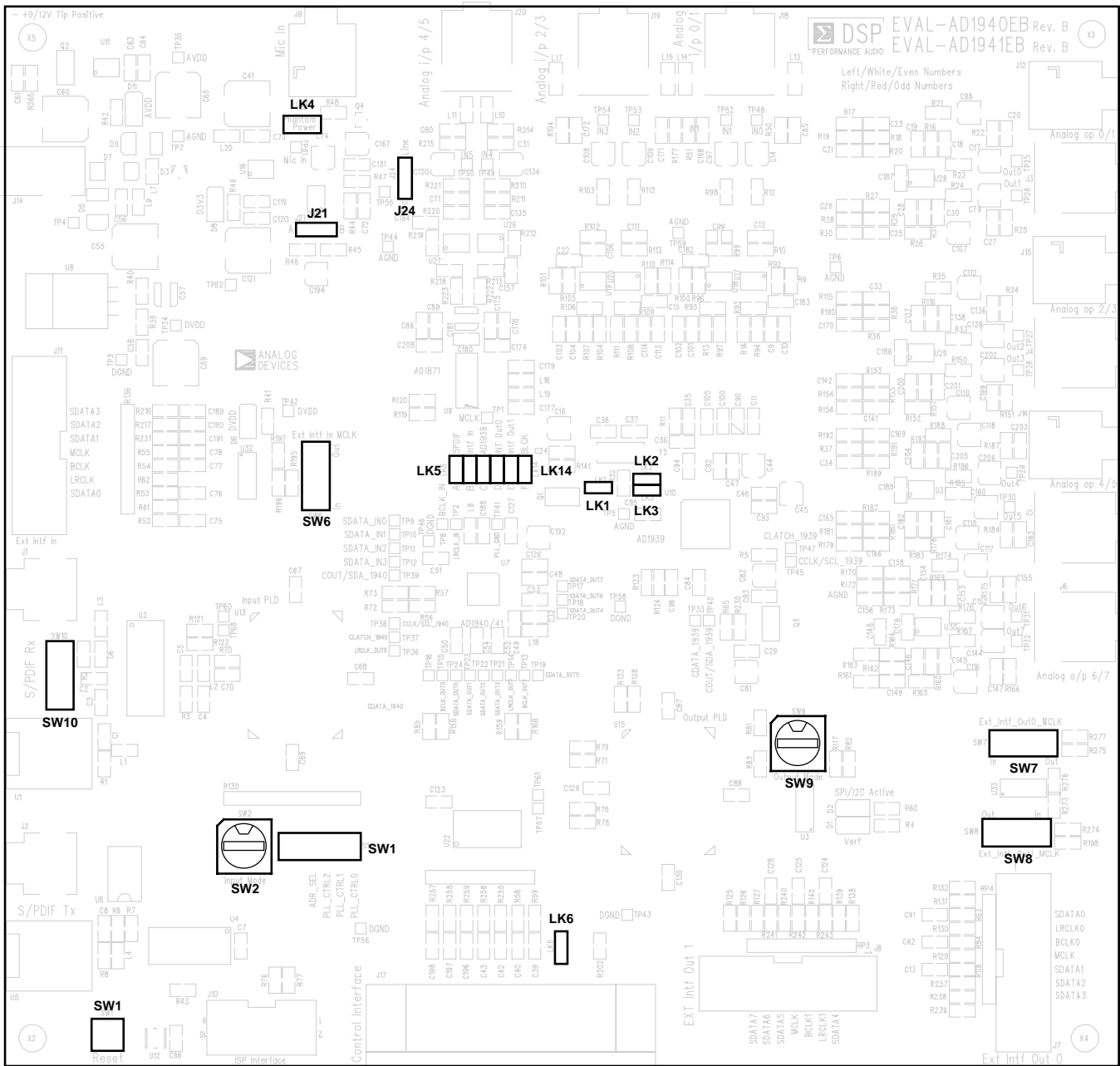# PCB DIAGRAMS
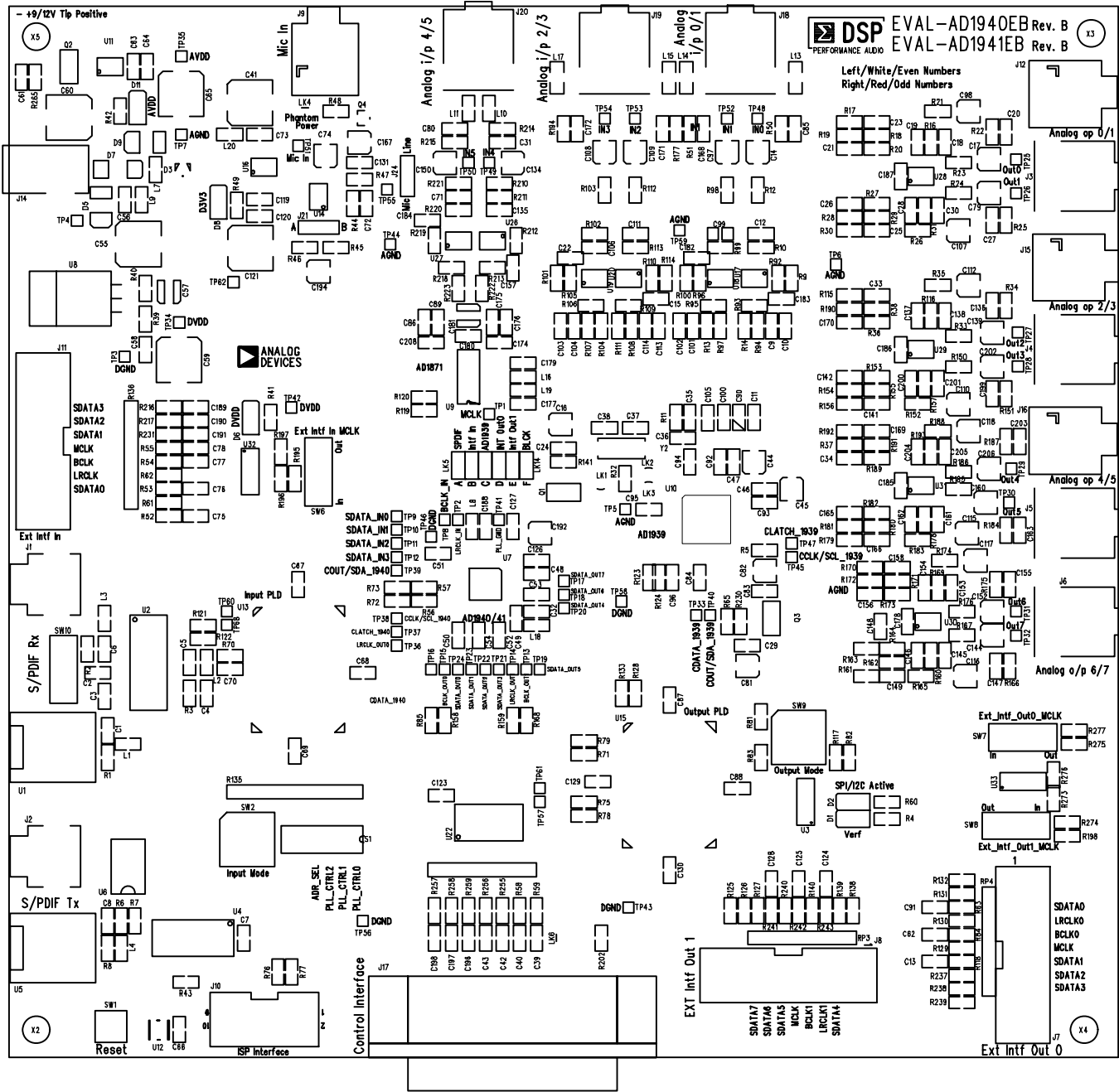
Figure 15. Top Layer Silkscreen
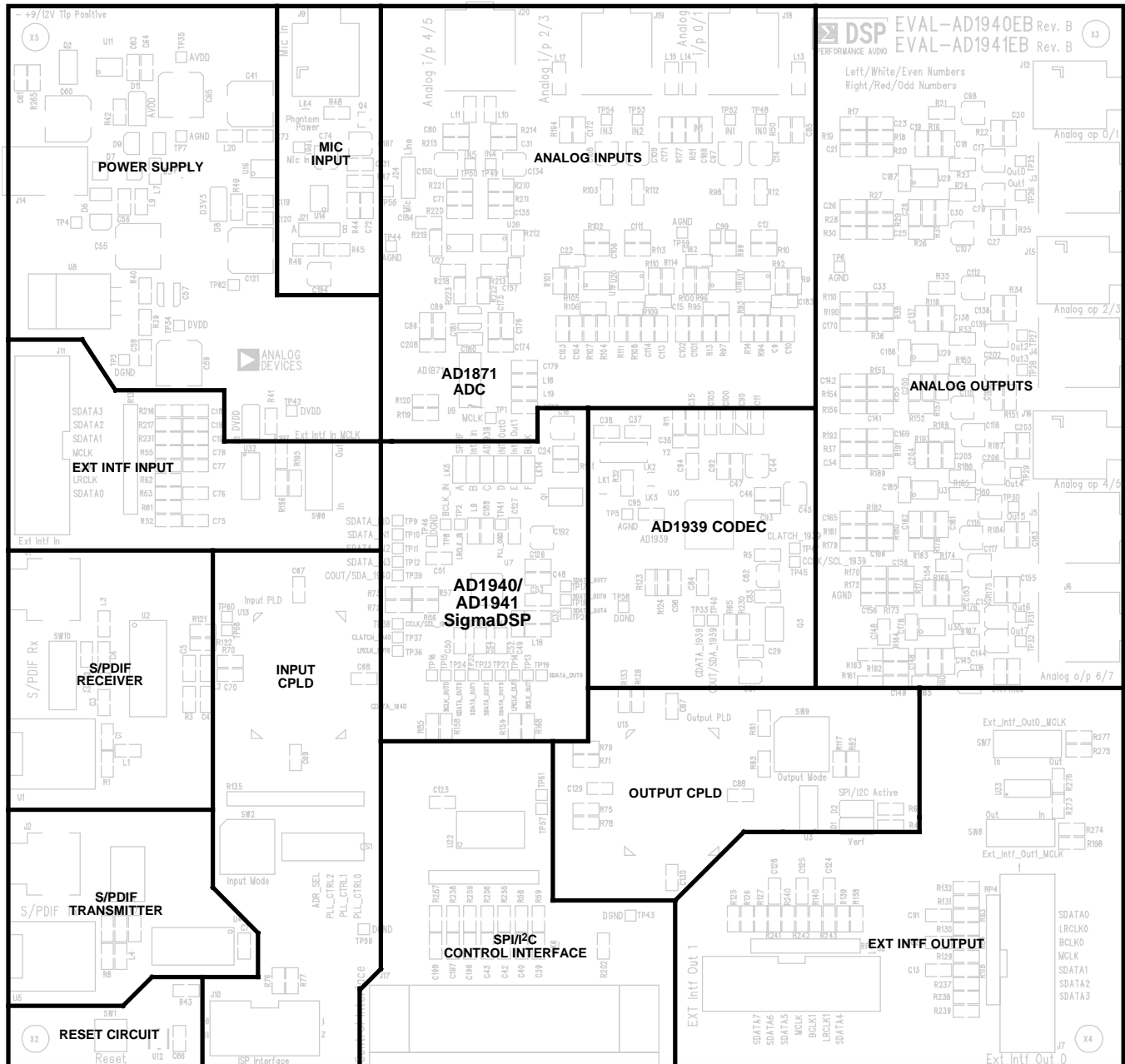
Figure 16. Evaluation Board Subsections

Figure 17. Evaluation Board Jumpers and Switches

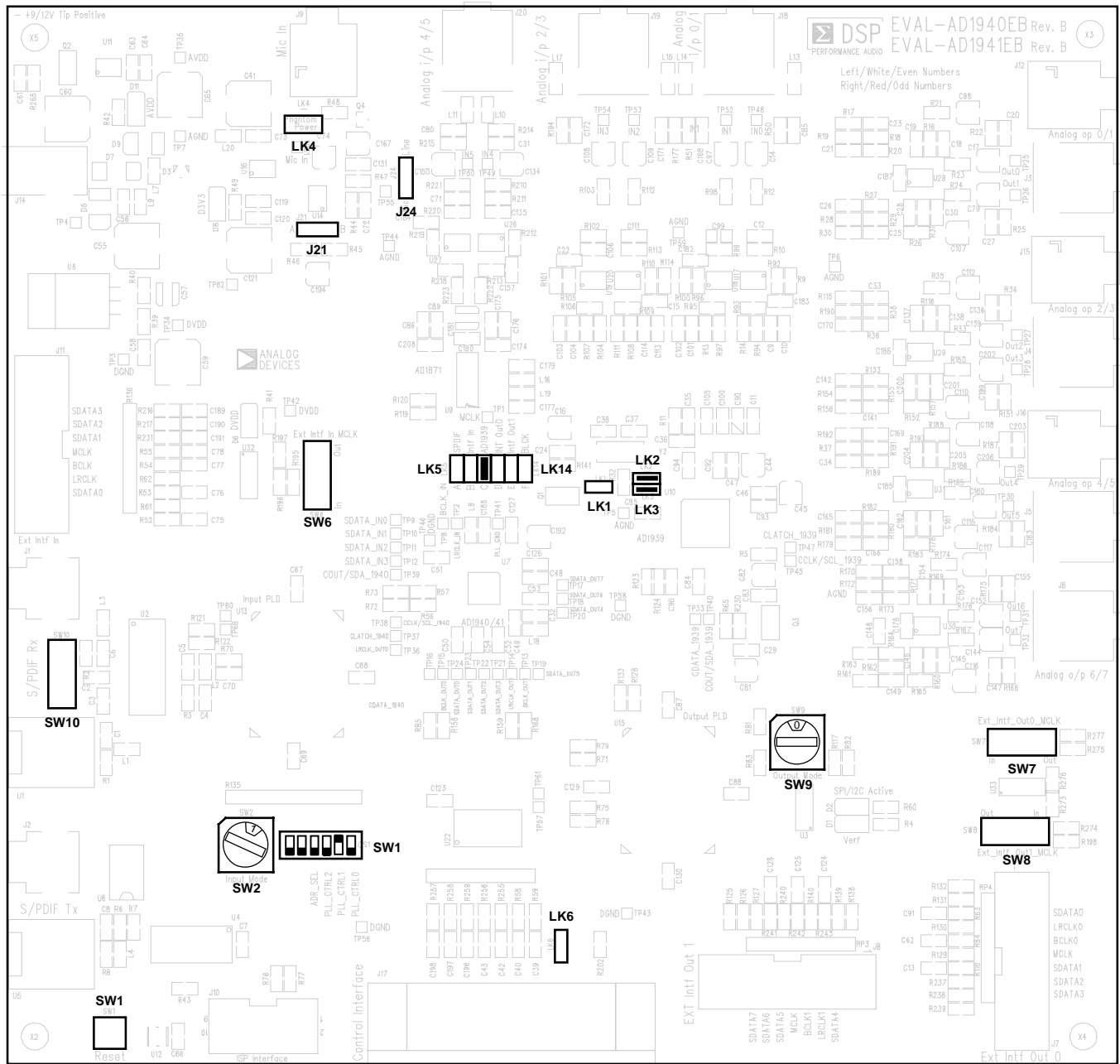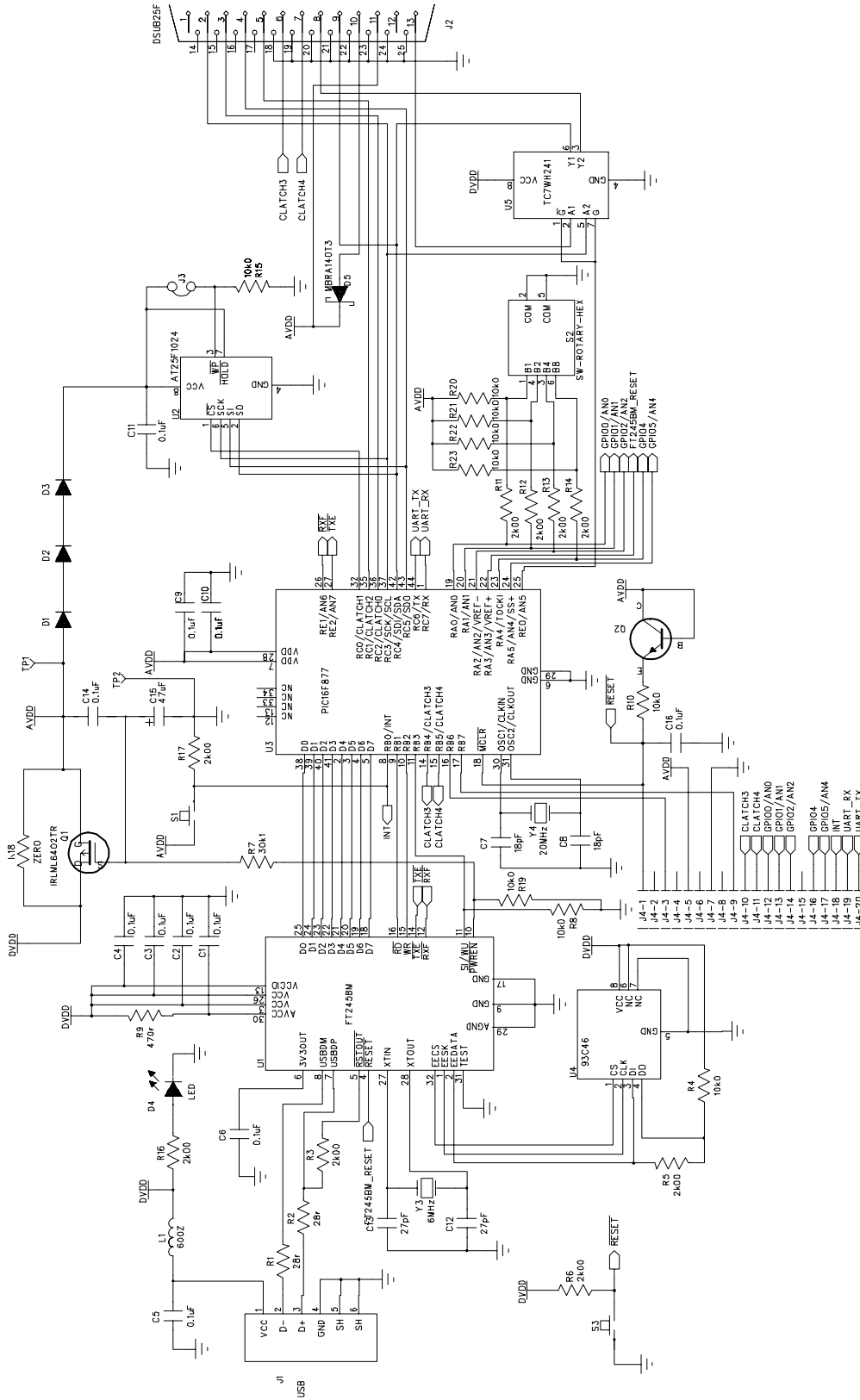Figure 18. Evaluation Board Jumper and Switch Default Settings

USB ADAPTER SCHEMATIC

Figure 19. USB Adapter Schematic

ORDERING INFORMATION

ORDERING GUIDE

Model	Description
Eval-AD1940EB	Evaluation Board
Eval-AD1941EB	Evaluation Board
Eval-ADUSB1	Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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